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DECISION-MAKING SIMPLIFIED: GENERIC RADAR PROCESSOR MAKES CHOOSING ALGORITHMS FOR DOPPLER MEASUREMENT A LITTLE EASIER

Selecting an algorithm to use in processing signals for a Doppler radar system could become easier with a signal processor developed by engineers at the Georgia Tech Research Institute (GTRI).

Principal Research Engineer Harold Engler and his colleagues have designed the Generic Doppler Processor, believed to be the first processor that emulates most known Doppler processing methods in real time using just one piece of hardware.

"One application would be for the radar designer," Engler said. "If you weren't sure how to configure a Doppler processor to make it work best for some application, you might want to use this equipment to experiment with different approaches and see which one works the best."

The Generic Doppler Processor could allow engineers to experiment with a variety of Doppler processing methods in real time using just one piece of hardware. (Color Slides/B&W Prints Available)

Doppler techniques are used to determine the speed of monitored targets. They also make targets appear more distinct from the background "clutter" that accompanies them on radar screens.

Variables affecting algorithm choice include the space and weight limits of the project under development, as well as what kind of hardware technology is available, Engler said. Currently, engineers choosing a Doppler algorithm must do the best they can with non-real-time computer simulations. They then build hardware prototypes of configurations they hope will work, try those out and modify them as needed.

Because of the uncertainty inherent in the design process, using Engler's

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real-time simulator could be less expensive than relying on current methods. The Generic Doppler Processor does not require building new hardware and is re-programmable, offering the flexibility of software, Engler said.

The flexibility of the Generic Doppler Processor also makes it useful in evaluating electronic countermeasures (ECM) techniques. The processor can be configured like each of the enemy systems the ECM will engage. This way ECM effectiveness can be evaluated against several enemy systems with only one piece of hardware.

"This generic processor actually combines what you get from a real-time prototype with the flexibility of non-real time computer simulations," he said. "You get two things at once."

Among the options the processor offers is use of digital hardware to simulate a bank of analog filters, each tuned to a different frequency. The analog equipment usually used to construct such a bank is bulky and awkward.

"It turns out that using the digital filters to simulate the analog filters may actually boost performance," Engler said. "The rejection of undesired signals can be superior to that available with Fast Fourier Transform (FFT) approaches."

A reduction in computations was the researchers' biggest challenge in developing the analog filter bank simulation, Engler said.

"While we knew how to do it, we didn't know a way to make it fast enough to complete the task in real time -- to keep up with what the filter would have to be doing if it were in a real radar," he said.

The researchers achieved the reduction by designing sequences of smaller filters that could do the job of one large one. This lowered computational demand by a factor of ten. The number of processing boards required was also reduced, thus dropping development costs.

Other processing methods the simulator offers include FFT and special correlator types.

The simulator uses an industrial PC chassis with one circuit board to drive the graphics display and ten additional boards to perform Doppler processing. A 386 central processing unit provides disk drive access and operator interface.

Now that they've demonstrated the concept, the researchers are seeking sponsorship in the development of an overall radar simulator. In addition, they are interested in exploring use of the same techniques to produce a generic processor for moving target indicator radars. This type of radar rejects signals from stationary objects by filtering.

This research was funded with monies from GTRI's Senior Technology Guidance Council, overseer of the GTRI internal research program. Additional Doppler simulator project members included Research Engineer Philip D. West, Graduate Research Assistants Mark D. Austin and Thomas R. Gardos, and Research Engineer Michael J. Cooper.

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A paper on this work, "The GTRI Generic Doppler Processor," was presented at a national symposium of the International Test and Evaluation Association (ITEA) Nov. 18-21, 1991, in Atlanta. An article, "Generic Doppler Processor Speeds Radar Analysis," appeared in the March 1991 issue of MICROWAVES AND RF.