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Research News

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PASSING THE TEST FOR CIRCUIT CARDS:
AUTOMATIC TESTING HELPS AIR FORCE
CUT MAINTENANCE COSTS & BOOST READINESS

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As military electronic equipment grows more complex, so do the problems of testing and maintaining it. Engineers at the Georgia Tech Research Institute (GTRI) have developed a set of software tools to automate and improve the testing of analog and hybrid circuit cards.

Developed for the U.S. Air Force, the Automatic Test Equipment Software Support Environment (ATESSE) will help boost aircraft readiness -- while reducing maintenance costs. The tools may eventually help designers produce electronic equipment that is easier to test.

"Trying to design test programs for mixed analog-digital circuits is a difficult problem," said Fred L. Cox, head of GTRI's Software Engineering Branch. "What we have put together is a set of tools that help test engineers develop their programs on computer-aided engineering workstations."

The ATESSE tools help engineers (1) simulate normal circuit performance, based only on design information, (2) determine proper tolerances for testing, (3) simulate the operation of faulty circuits, (4) automatically produce software code for test programs based on flow chart information, and (5) compare circuit simulations to actual circuit operation.

Test engineers face a complex problem: detecting, isolating and replacing faulty components in malfunctioning circuit cards. With the rising cost of circuit cards and the components on them, the Air Force would like to replace only the malfunctioning components.

But isolating those parts can be difficult, particularly in analog circuits, where the number of ways faulty behavior can be expressed is fairly large. "It's very difficult for an engineer to understand the full range of possible fault behaviors for a complex analog circuit," Cox explained.

To find the faulty part, engineers calculate what tolerances are acceptable in the circuit's electronic operation, then design a sequence of diagnostic tests designed to single out the malfunctioning parts.

"The test sequence is normally documented in a flow chart," Cox explained, "and once that design is done, the engineer translates it into a program written in the ATLAS language."

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But ATLAS can be difficult to use, particularly for electronic engineers not accustomed to programming.

To help them, the ATESSE can convert a test flow chart directly to ATLAS code, eliminating the need for engineers to learn ATLAS programming. Cox believes that will help engineers produce better test programs -- with fewer bugs.

"The engineer can focus his competence on the testing rather than the programming," he said. "It reduces the amount of time that it takes to write the code, and eliminates many of the errors that are introduced through the manual coding process."

The ATESSE also helps calculate the tolerance values, combining specifications from the various components involved and the test equipment itself. The software can even perform its simulation at different levels of circuit abstraction, reducing simulation time.

Georgia Tech recently received additional funding from the Air Force's F-16 System Program Office and the Warner Robins Air Logistics Center to begin Phase III of the ATESSE project. During this stage, Cox hopes to partially automate the test program development process, using artificial intelligence to design the test sequence from a schematic diagram of the circuits and basic performance data.

Because of the circuit card's complexity, engineers often overlook test opportunities that could help pinpoint problems. Cox expects that an automated system could detect significantly more testing opportunities, producing a more efficient test program able to pick out a higher percentage of electronic faults with a smaller investment of time.

What will this mean for the Air Force?

"We believe that the ATESSE will pay for itself very rapidly during the test program development cycle," said Cox. "But the largest cost savings should come during the maintenance cycle because the ATESSE can eliminate a large portion of the errors that result in maintenance cost. We expect higher quality software, lower development costs, better productivity of the test engineers, and significantly reduced maintenance costs."

Ultimately, Cox hopes to extend the ATESSE to help design engineers, because he believes analog circuit designers need the simulation capability. Also, he noted, if designers were more aware of testing needs, they could produce circuits that are easier to test -- and cheaper to repair.

"One of the problems test engineers have is that although a given circuit design may work very well, it may be difficult to test," he said. "We would like to take some of the concepts we are developing for testing and incorporate them into the design environment. We should be able to give the designers immediate feedback on the testability of their designs and suggestions for improving them."

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